What Is Claimed Is

PATENT CLAIMS

1. Computer-supported method for partitioning an electrical circuit,

- whereby the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit,

- whereby edges of the graph have weighting values allocated to them with which a required calculating outlay for determining electrical descriptive quantities for elements of the electrical circuit that are represented by the respective edge is described,

- whereby a first sum value of the weighting values of the edges is calculated for edges coupled to one another and, in further iterations, the first sum value is respectively formed upon addition of at least one further edge until the respectively calculated, first sum value is greater than a prescribable, first threshold,

- whereby a partition of the electrical circuit is formed by the edges taken into consideration in the formation of the first sum value,

- whereby the following steps are implemented for at least a part of the remaining edges that do not lie in the partition and that are coupled to at least one edge of the partition:

-- a second sum value is determined that derives from the sum of the first sum value and at least one weighting value of at least one remaining edge,

-- when the second sum value is smaller than a prescribable second threshold, and

-- when a plurality of edges that were taken into consideration in the formation of the second sum value that are coupled to edges that were not taken into consideration in the formation of the second sum value is smaller than a plurality of edges of the partition that are coupled to the remaining edges, then

-- the remaining edge is allocated to the partition and the second sum value is allocated to the first sum value, and

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- whereby the partition is formed by the edges taken into consideration in the formation of the second sum value.

2. Method according to claim 1, whereby a grouping of elements of the electrical circuit for which it is respectively found that these elements are allocated in common to a partition is implemented at the beginning of the method.

3. Method according to claim 2, whereby at least one of the following rules is applied in the grouping of the elements of the electrical circuit:

- elements of a controlled source, at least a controlling element and the controlled source, are allocated in common to a partition,
- connecting loops in the electrical circuit that only contain at least one voltage source and at least one counter-inductance are allocated in common to a partition,
- no shorts dare arise due to the partitioning.

4. Method according to one of the claims 1 through 3, whereby a plurality of edges of the graph have a common weighting value allocated to them.

5. Method according to one of the claims 1 through 4, whereby the graph of the partition is imaged onto the electrical circuit, whereby the partition comprises the elements of the electrical circuit corresponding to the implemented partitioning.

6. Method according to one of the claims 1 through 5

- whereby a plurality of partitions are formed by multiple implementation of the method, and
- whereby the electrical descriptive quantities for the elements of the electrical circuit are determined for each partition, whereby at least a part of

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the partitions is processed in parallel on the plurality of computers and/or processors.

7. Method according to claim 6, whereby the parallel processing of the partitions is centrally controlled.

8. Method according to claim 7, whereby at least a part of the partitions are centrally controlled in such a way that all terminals of the respective partition are coupled only to a central control unit and, thus, a communication of data ensues only between the central control unit and at least the part of the partitions.

9. Method according to claim 8, whereby a voltage source is additionally allocated at least to a part of the terminals of the respective partition, the value of said additional voltage source to be predetermined by the central control unit during the determination of the electrical descriptive quantities.

10. Method according to claim 9, whereby a resistor is additionally allocated at least to a part of the terminals of the respective partition.